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TRIMON C250

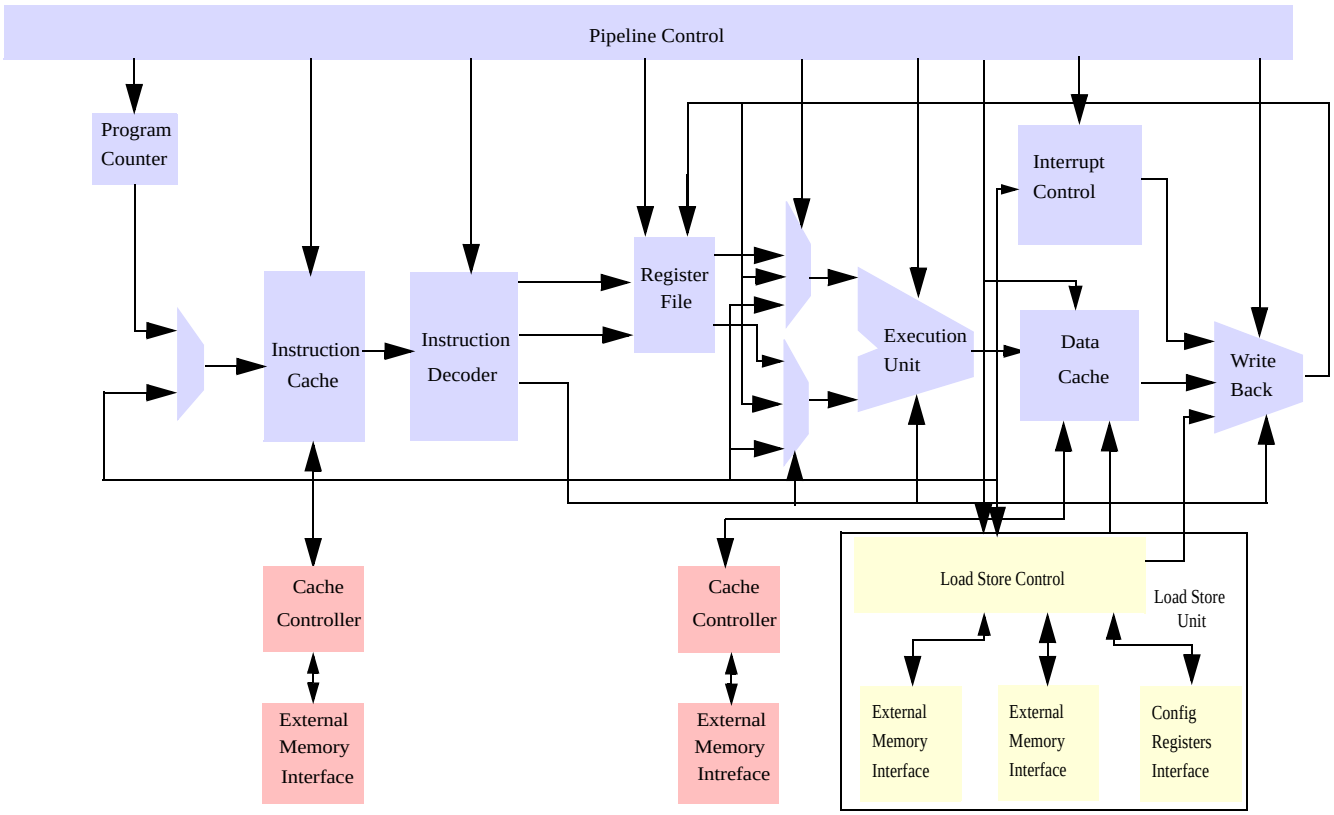
Feature Specification

- High-Performance cached MIPS I Instruction Set Compatible Processor Core
- Extensions and accelerators to the Instruction Set can be added
- Two Staged Fully Pipelined Instruction Cache. The associativity and size of Instruction Cache are configurable based on application requirements.
- Two Staged Fully Pipelined Data Cache. The associativity and size of Data Cache are configurable based on application requirements.
- 250MHz Operating frequency in 0.18um TSMC process
- Operating frequency can be increased if necessary.
- 0.3mm**2 in 0.18 TSMC process without memories
- 1.5mm**2 in 0.18 TSMC process including memories
- Support for 3 external indepenedent memory systems, memory load-store units included.
- The External Memory Interface is scalable and it can support different partitioning.
- Gaskets can be added to support buses like AMBA etc.
- RS232 based software debugger (optional)
- Ideal for SoC data-communication, packet processors, packet classification engines and embedded applications.

The TRIMON 250 IP Package

- TRIMON C250 Verilog RTL
- Verilog Testbench
- Verification Environemnt, scripts and tools
- Assembler development toolchain
- “C” development toolchain
- Micro-Kernel program management firmware

Block Diagram



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