TRIMON T250

High-Performance Multi-Threaded Procesor Core

Feature Specification

- High-Performance MIPS I Instruction Set Compatible Processor Core

- Extensions and accelerators to the Instruction Set can be added

- Hardware multi-threaded support

- 4 hardware threads supported (scalable to 8, 16, 32)

- Dedicated instruction and data thread context storage

- Single cycle thread swap

- 16kB Instructiom Memory (IMEM). IMEM size can be changed based on application requirements.

- 16kB Data Memory (DMEM) DMEM size can be changed based on application requirements.

- 250MHz Operating frequency in 0.18um TSMC process

- Operating frequency can be increased if necessary.

- 0.3mm**2 in 0.18 TSMC process without memories

- 1.5mm**2 in 0.18 TSMC process including memories

- Support for 3 external indepenedent memory systems, memory load-store units included.

- The External Memory Interface is scalable and it can support different partitioning.

- Gaskets can be added to support buses like AMBA etc.

- RS232 based software debugger (optional)

- Ideal for SoC data-communication, packet processors, packet classification engines and embedded applications.

The TRIMON T250 IP Package

- TRIMON 4TR250 Verilog RTL

- Verilog Testbench

- Verification Environemnt, scripts and tools

- Assembler development toolchain

- "C" development toolchain

- Micro-Kernel program management firmware

Block Diagram