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SOC PLATFORM

Feature Specification

- Multi-purpose SoC Platform
- Multiple processor cores support for scalable computing performance
- Configurable Instruction and Data Cache sizes
- Cached and Code-swapped Processor Cores support
- Configurable number of debug or general purpose communication interfaces
- General purpose decoded register space for attaching variety of specialized cores, encryption/decryption engines, DSP cores, peripheral controllers, bus sockets and others.
- Support for local LSU memory interconnect
- Support for remote/external memory interconnect through the bus interconnect system.
- Support for secondary bus interconnect for better data bandwidth allocation and management.
- 250MHz Operating frequency in 0.18um TSMC process
- Ideal for SoC data-communication, digital communications, storage, consumer, packet processors, packet classification engines and general purpose embedded applications.

The SOC PLATFORM Package

- SoC Blocks Verilog RTL
- SoC Blocks Verilog Testbench
- SoC Blocks Verification Environment, scripts and tools
- Assembler development toolchain
- “C” development toolchain
- Micro-Kernel program management firmware

Block Diagram