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DDR DRAM Controller

High-Performance Universal DDR DRAM Memory Controller Core

Feature Specification

- Support of AMBA AXI and AMBA AHB interfaces
- Read and write FIFOs with configurable length
- Configurable master system and memory bus width
- Reordering function for maximum bandwidth
- Supports DDR1, DDR2, FCRAM, RLDRAM memories
- Fully programmable DRAM parameters
- Dynamically reconfigurable memory burst length
- Fully software based memory initialization and configuration
- Built in self test
- ECC - optional

The DDR DRAM Controller IP Package

- DDR Controller Verilog RTL and Netlist
- Full controller specification
- Verilog Testbench
- Test plan documentation
- Verification Environment, scripts and tools
- Primetime timing scripts
- Synopsys synthesis scripts

Block Diagram